Experimental characterization of the 192 channel Clear-PEM frontend ASIC coupled to a multi-pixel APD readout of LYSO:Ce crystals

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A B S T R A C T

In the framework of the Clear-PEM project for the construction of a high-resolution scanner for breast cancer imaging, a very compact and dense frontend electronics system has been developed for readout of multi-pixel S8550 Hamamatsu APDs. The frontend electronics are instrumented with a mixed-signal Application-Specific Integrated Circuit (ASIC), which incorporates 192 low-noise charge pre-ampifiers, shapers, analog memory cells and digital control blocks. Pulses are continuously stored in memory cells at clock frequency. Channels above a common threshold voltage are readout for digitization by off-chip free-sampling ADCs. The ASIC has a size of 7.3 × 9.8 mm² and was implemented in a AMS 0.35 μm CMOS technology. In this paper the experimental characterization of the Clear-PEM frontend ASIC, reading out multi-pixel APDs coupled to LYSO:Ce crystal matrices, is presented. The chips were mounted on a custom test board connected to six APD arrays and to the data acquisition system. Six 32-pixel LYSO:Ce crystal matrices coupled on both sides to APD arrays were readout by two test boards. All 384 channels were operational. The chip power consumption is 660 mW (3.4 mW per channel). A very stable behavior of the chip was observed, with an estimated ENC of 1200 ± 1300 e− at APD gain 100. The inter-channel noise dispersion and mean baseline variation is less than 8% and 0.5%, respectively. The spread in the gain between different channels is found to be 1.5%. Energy resolution of 16.5% at 511 keV and 12.8% at 662 keV has been measured. Timing measurements between the two APDs that readout the same crystal is extracted and compared with detailed Monte Carlo simulations. At 511 keV the measured single photon time RMS resolution is 1.30 ns, in very good agreement with the expected value of 1.34 ns.

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1. Introduction

Nowadays, PET is recognized as a powerful imaging technique for the detection of tumors in oncological diseases. 18F-FDG PET imaging allows to map areas of localized increase of metabolic activity that may indicate the presence of a neoplasm before morphological changes are detected by other imaging modalities. This is the example of breast cancer where PET is more efficient to detect lesions and to distinguish benign findings from malign formations in comparison with standard mammography techniques (X-ray). 18F-FDG PET for the evaluation of breast cancer has started in 1989, resulting in a published study on 17 breast cancer patients in advanced stage [1]. Subsequent analysis of combined clinical trials with 259 patients has yield a sensitivity (true positive/total positive) of 92% and specificity (true negative/total negative) of 94%. Almost all exams were carried out with a whole-body PET scanner, which may justify that although sensitivity was about 90% for tumors larger than 2 cm [2] it decreases to 25% when lesions with diameters less than 1 cm are considered. The decrease in small breast tumors detectability performance is
mostly due to the suboptimal spatial resolution of current whole-body PET scanners [3]. Spatial resolution in whole-body PET is limited to 0.5–1 cm which has prevented the use of PET imaging exclusively for breast cancer screening purposes [4].

At the light of the current limitations of whole-body PET scanners for breast cancer detection and motivated by the fact that PET facilities have a low patient turnover and high cost for mass screening, in terms of the required equipment and personnel, dedicated specially tailored PET systems have been advocated [3,5,6]. Such devices, generally named Positron Emission Mammography (PEM), are designed to image the breast region by favoring high-resolution and detection sensitivity over the general purpose of whole-body scanners. The design goals for PEM instruments include short imaging time, high spatial resolution, improved diagnostic specificity to reduce the need for surgical biopsies and confident definition of tumor prior to biopsy or other surgical options.

The geometry of a dedicated PET scanner for mammography should provide a large angular coverage by placing the detectors as close as possible to the breast. The photodetector elements should be based on high-Z stopping power materials, with an adequate thickness and an enhanced photoelectric interaction probability, while the readout electronics should not contribute to degradation on the spatial resolution. When planar detectors are located close to the object under examination, the thickness of the photon detection sensitive material may introduce deterioration on the spatial resolution due to the so-called parallax effect. This effect originates from the fact that conventional PET scanners are not capable of determining the position of the photon interaction along the detection material.

The parallax error becomes more severe as the distance between the opposing detection elements decreases, or the angular range of accepted events increases [6,7]. Therefore, it is desirable that the readout method should be compatible with the estimation of the depth-of-interaction (DOI) along the crystal longitudinal dimension. In addition, and since the large fraction of the injected dose would be located outside the field-of-view (FOV), namely in the heart, liver and torso, the detector should have a low deadtime at channel level and a good time measurement capability to minimize the accidental coincidences due to the single photon background rate. An efficient data acquisition system, capable of on-line single event rejection with a minimum processing deadtime is required, lowering the data rates to a level compatible with general purpose high-speed data links and off-the-shell mass storage systems.

The Clear-PEM scanner has being developed by the Portuguese PET Consortium under the framework of the Crystal Clear Collaboration [8–10]. The major technical specifications are presented in Table 1. The detector assembly is based on two detecting planar heads, with a $17 \times 15 \text{ cm}^2$ FOV [9]. The detection heads are mounted on a robotized mechanical system, enabling the exam of both breasts, one at a time, as well as the axillary lymph nodes. The Clear-PEM scanner adopts Lu$_2$Y$_2$SiO$_5$ (LYSO:Ce) [11] scintillator crystals with individual dimensions of $2 \times 2 \times 20 \text{ mm}^3$. The traditional readout based on photomultipliers is replaced by multi-pixel avalanche photodiodes (APD). Due to its compactness, it is possible to read each single crystal with one APD pixel on each ends, and to use the relative amplitude of the two signals to estimate the longitudinal coordinate of the interaction point [12,13]. This solution named “double readout” cannot be easily implemented in conventional whole-body ring or planar PET scanners, since the amount of nonactive material (electronics and photomultipliers) placed between the anatomic region under examination and the crystals would lead to an unacceptable decrease of the detection efficiency due to the reduction of the solid angular coverage and additional attenuation of the incoming photons.

The individual 1:1 crystal-pixel APD coupling scheme leads to 12,288 channels, with a density at about 13 channels per centimeter square. The limited available space in the patient port to place the cooling equipment, required in face of the influence of temperature on the APD performance ($-2.5\% / \text{K}$ at gain $M = 50$ and increase of dark current by a factor of 2 per 11 K) demand that all the processing electronics must have a strict limited power consumption and thermal dissipation budget. This and the low gain ($50–200$) of the APDs has lead to the development, for the Clear-PEM scanner, of a family of specifically tailored low-noise VLSI chips. The output pulses are digitized by free-sampling ADCs. The most demanding data processing task is concentrated in the off-detector electronics, based on a reconfigurable FPGA fabric [10], which implements a first-trigger (L1) decision. The online trigger extract the pulse features (energy and time) needed for a two-photon coincidence decision, discarding out-of-time single photons. The data rate to be stored in mass storage elements can reach up to 250 MByte/s [14,15]. Accepted events are revalidated by a second trigger (L2), software based on a multi-core server, that re-process the datastream with more complex algorithms for the determination of energy, time, DOI and assignment of the crystal of first interaction, for events with multiple hits due to in-detector Compton. Second-level accepted triggers are then stored and used as input for the image reconstruction algorithms.

### Table 1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of LYSO:Ce crystals</td>
<td>6144 ($2 \times 20 \text{ mm}^3$ each)</td>
</tr>
<tr>
<td>Number of crystal matrices</td>
<td>192</td>
</tr>
<tr>
<td>Number of electronic channels</td>
<td>12 288</td>
</tr>
<tr>
<td>Number of multi-pixel APDs</td>
<td>384</td>
</tr>
<tr>
<td>Number of multi-channel ASICs</td>
<td>64</td>
</tr>
<tr>
<td>Frontend to L1 bandwidth</td>
<td>78 (50 MHz) to 156 Gbps (100 MHz)</td>
</tr>
<tr>
<td>L1–L2 bandwidth</td>
<td>400 (50 MHz)–800 MB/s ($100$ MHz)</td>
</tr>
<tr>
<td>Number of LORs</td>
<td>37 748 736</td>
</tr>
<tr>
<td>Scintillator volume</td>
<td>491.52 cm$^3$ (≈ 3.5 kg)</td>
</tr>
<tr>
<td>Active surface area</td>
<td>$17 \times 15 \text{ cm}^2$ (≈ 13 channels/cm$^2$)</td>
</tr>
<tr>
<td>Separation distance</td>
<td>5–40 cm</td>
</tr>
<tr>
<td>$\phi_{\text{total \ angle \ at \ 10 \ cm \ separation}}$</td>
<td>0.47</td>
</tr>
</tbody>
</table>

2. The Clear-PEM frontend electronics

The Frontend Electronics System, physically located on the detector heads, performs signal amplification, channel selection and analog multiplexing, analog to digital conversion and parallel-to-serial translation. The frontend electronics block is, in several aspects, one of the most sensitive and critical sub-system of the Clear-PEM detector. The frontend chip must be low-noise, due to the initial reduced charge at the amplifier input, which for a 511 keV photon energy deposit is around 30 fC (maximum value), or a peak current around 0.75 nA, assuming a LYSO:Ce 42 ns time constant [11]. The frontend chip should amplify this charge by about three orders of magnitude, while complying with the low-power dissipation requirements, compatible with a compact cooling system. A cooling system is required since the LYSO:Ce light yield and APD gain are inversely dependent on the temperature. The collected charge at the input is constrained by the S8550 APD gain, crystal-APD pixel size mismatch, and to the fact that in each crystal the light is split by two photosensors. Since the Frontend Boards (FEBs), in which the Application-Specific Integrated Circuits (ASICs) are mounted, have a mixed analog–digital environment, special care is needed regarding the
correct conditioning of the digital, large amplitude, high-frequency signals from clocks and other periodic signals. Noise pickup in the PCB traces that connect the APD outputs to the frontend chips must also be minimized by keeping the trace length as small as possible of about a few millimeters.

The Clear-PEM ASIC is designed for the readout of Hamamatsu S8550 multi-pixel APD. Specifications for this APD are summarized in Table 2 and in Refs. [16–18]. The noise specification of the ASIC amplifiers is a function of the energy and time resolution requirements. An equivalent noise charge (ENC) of around 1000–1500e− RMS contributes less than 2% to the energy resolution, which at 511 keV is dominated by the LYSO:Ce intrinsic and photostatistics terms to the energy resolution [19]. For a signal peaking time of 30–40 ns, this noise level implies a RMS time resolution of the order of 1 ns. To achieve peaking times of this order, a fast amplifier response (15–20 ns) is required, roughly half of the LYSO:Ce decay time. In this circumstances only 40–50% of the input charge contributes to the amplitude of the output pulse. In overall, a gain of 30–40 mV/fC (defined here as the gain of the output pulse in response to a Dirac-like charge input) is required. Power and cabling constrains required that some form of multiplexing and zero suppression should be implemented in the chip, keeping to a minimum the number of output channels. The number of output channels in a scanner with crystals with small cross-section has to be chosen adequately in order to avoid significant losses of information that could compromise the detection sensitivity of two-photon events in coincidence. Monte Carlo results show that in the case of Clear-PEM about 53% of all coincidences will have two or more crystal hits in a given detector head per event [9]. Therefore, the number of output channels for the frontend ASIC should be 2, still allowing for the readout of multi-Compton interactions (more than 2) in the scanner if the event is readout by two different ASIC regions (“Trigger Cell”) (see Section 3.1).

The need to readout 12 288 channels placed in a very constrained space demands that the frontend ASIC has an unprecedented level of integration. The adopted architecture consists on 192 amplifiers and shapers integrated in a circuit chip, which receive the signals generated by up to six APD arrays (Fig. 1 and Table 3). At every clock cycle the input signals are sampled and the corresponding charge stored in the capacitor array with a depth of 10 cells. In parallel, at the clock frequency, each of the sampled signals is compared to the $V_{th}$ voltage threshold, followed by digital logic to determine the channels above threshold. The threshold is adjustable externally, by a 12-bit precision DAC, and is the same for all 192 channels. If one sample in one input channel is found above threshold, this input channel is multiplexed to the first free output channel together with a digital channel identifier that establishes the correspondence with the input APD channel. The digital identifier has a 10-bit length. The first bit signals the start of a transmission, and the following 8-bit encode the APD channel. The last bit is reserved to signal a output channel overflow condition. The connection is maintained open for 10 clocks, for the transmission of the 10 consecutive samples. The set of the 10 samples is called an analog dataframe [10]. Above two signals over the common threshold, the third input signal is ignored, and the error bit is asserted. The error code (overflow condition) is used by the L1 trigger system to discard the received data. LVDS signaling is used for the external clock that drives the ASIC, as well as for the digital outputs to reduce the

**Table 2**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size</td>
<td>1.6 mm x 1.6 mm (x32 pixels)</td>
</tr>
<tr>
<td>Pixel pitch</td>
<td>2.3 mm</td>
</tr>
<tr>
<td>Window type</td>
<td>0.5 mm thick epoxy resin</td>
</tr>
<tr>
<td>Peak sensitivity wavelength</td>
<td>600 nm</td>
</tr>
<tr>
<td>Quantum efficiency at 365 nm</td>
<td>50–58%</td>
</tr>
<tr>
<td>Quantum efficiency at 420 nm</td>
<td>72–76%</td>
</tr>
<tr>
<td>Gain</td>
<td>50–200</td>
</tr>
<tr>
<td>Polarization bias</td>
<td>400–500 V</td>
</tr>
<tr>
<td>Gain gradient at $M = 50$</td>
<td>3.0%/V</td>
</tr>
<tr>
<td>Gain gradient at $M = 100$</td>
<td>5.8%/V</td>
</tr>
<tr>
<td>Gain gradient at $M = 200$</td>
<td>13.4%/V</td>
</tr>
<tr>
<td>Dark current</td>
<td>2–4 nA (per pixel at gain $M = 50$)</td>
</tr>
<tr>
<td>Capacitance</td>
<td>10 pF (per pixel at gain $M = 50$)</td>
</tr>
</tbody>
</table>

**Table 3**

<table>
<thead>
<tr>
<th>Clear-PEM frontend ASIC target specifications.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Number of channels</td>
</tr>
<tr>
<td>$T_{peak}$ (APD charge input)</td>
</tr>
<tr>
<td>$T_{peak}$ (Dirac test pulse)</td>
</tr>
<tr>
<td>Noise</td>
</tr>
<tr>
<td>Multiplexing level</td>
</tr>
<tr>
<td>Output analog channels</td>
</tr>
<tr>
<td>Output digital channels</td>
</tr>
<tr>
<td>Input clock range</td>
</tr>
<tr>
<td>Die area</td>
</tr>
<tr>
<td>Number of input pads</td>
</tr>
<tr>
<td>Number of I/O and control pads</td>
</tr>
<tr>
<td>Number of power supply pads</td>
</tr>
<tr>
<td>Supply voltage</td>
</tr>
<tr>
<td>Power</td>
</tr>
<tr>
<td>Process</td>
</tr>
</tbody>
</table>

![Fig. 1. Functional representation of the Clear-PEM frontend ASIC.](image-url)
risk of coupling digital noise to the amplifier inputs. The target chip power consumption is about 600–700 mW. The differential analog dataframes are digitized by free-sampling dual 10-bit ADCs with differential inputs, clocked at a fixed phase shift in relation to the ASIC input clock. The phase shift is controlled by the ASIC through a clock skew delay. The digital data are then carried over a 40-bit bus, plus the channel identifiers, to a LVDS “Channel Link” 48:8 bit chip that serializes the data. After the contribution from the ADCs, “Channel Link” serializer and LVCMOS/LVDS logic level converters, assuming a 50 MHz master clock, is taken into account the total power consumption per detector head is 55 W.

In the course of the construction of the Clear-PEM scanner, three ASIC versions were produced. The first version was a multi-purpose development chip which includes in the same die several functionalities: 32 input channel amplification circuit with individual access points; two fully instrumented channels with amplification and digital control circuit, but also with individual access points; a complete 32:2 amplification/multiplexing circuit. Experimental tests have allowed to successfully validate the analog memory and digital controls up to 100 MHz working frequency, but the amplifier was found to require changes [20]. This was addressed in the second prototype version, which included a revised version of the amplifiers. Several experimental tests and quality control testbenches were carried out that demonstrate that all major requirements were successfully achieved. The measured gain was 23 mV/FC. The successful conclusions of the characterization tests of the second prototype allowed to start the development of the final ASIC fully instrumented with 192 input channels. About 170 ASICs were produced by Europratice in AMS (Austriamicrosystems) 0.35 μm CMOS process. In Fig. 2 a closeup photograph of a die directly bonded on a test board PCB is shown.

3. Experimental results

3.1. Characterization setup

The experimental testbench that was setup to characterize the frontend chip uses the different electronic sub-systems developed for the Clear-PEM scanner. A test board for the ASICs was designed with six layers, having components on both the top and bottom layers (Fig. 3). Careful layout policies of ground planes for analog and digital were followed in order to avoiding coupling of digital noise with the analog section of the ASIC as well as with the APD HV bias supply lines. The test board has all the main components of the final FEBs as well as some testability features like the capability to disable each one of the six blocks of 32 amplifier channels by putting all the amplifiers inputs at the reference voltage (+3.3 V). The ASIC die is directly bonded into the PCB. The board has six low-profile connectors in which the S8550 APDs are plugged-in. The differential analog outputs of the ASIC are routed to a ±1 V differential dual 10-bit ADC. The differential LVDS ASIC digital outputs that carry the digital identifier are translated to a
+3.3 V LVCMOS level and fed in parallel with the ADC LVCMOS digital outputs to the serializer chip. The differential analog and digital outputs are also available in eight LEMO00 single-ended connectors with a 50 Ohm adaptation, allowing the direct reading of the ASIC activity in an oscilloscope. The input clock, for the tests described in this paper was set to 50 MHz. The system clock is generated in the L1 data acquisition electronics TGR/DCC board (Fig. 6) and fanout by a dedicated board that translates the LVPECL clock to LVDS level, before arrival to the test board (Fig. 4). The output LVDS clock of the ASIC is then converted to LVCMOS clock and is used to drive the ADC and the serializer chip. In order to guarantee that the ADCs will sample the analog pulse in a stable region instead of the sharp transitions, some trial-and-error trials were carried out by changing the resistor that controls the ASIC clock output skew in relation to the analog samples. A delay of about 4 ns was used for the reported tests. In the Clear-PEM scanner heat dissipated by the ASICs, ADC and serializers is removed by means of water cooled dissipation plates in thermal contact with the FEBs. In the tests reported in this paper, the ASICs dies were covered by a temporary glass cover since the step of covering the die with a thermally conductive epoxy adhesive (glob-top) had not been performed. This has prevented the usage of a suitable cooling system. Instead cold air was directed to the board avoiding the uncontrolled heating of the APDs. Using this approach the temperature measured under the PCB region underlying the APDs was 24–26 °C. Two test boards were used to readout the six Hamamatsu S8550 APDs from each side of a set of six LYSO:Ce crystal arrays, each one with 32 pixels, forming a structure called “Trigger Cell”, which defines the basic readout element in the Clear-PEM scanner (Figs. 4 and 5). The serialized
output of the test boards was connected to one of the DAQ Boards of the L1 trigger (Fig. 6). Acquisitions using external $^{22}$Na, $^{137}$Cs sources and LYSO:Ce background from $^{176}$Lu radioisotope were done. $^{176}$Lu is present in 2.6% fraction mass of natural occurring Lutetium with a lifetime of $3.73 \times 10^{10}$ years. The typical decay rate is 300 decays per cubic centimeter of LSO:Ce $^{[21,22]}$. The common threshold $V_{th}$ was initially set at 1.55 V (equivalent to $\approx 120$ keV), 56 mV above the chip baseline (1.49 V). The trigger was operated in single photon mode, which means that all accepted events above the L1 energy threshold (set at 200 keV) are readout to the data acquisition server. Raw data, composed by the collected dataframes, channel identifiers, 17-bit timetag calculated by the DAQ on-board FPGAs (9-bit coarse timetag taken from the system clock and a 8-bit timetag computed from the digital time filter $^{[23]}$), were reprocessed by the L2 trigger and stored in a ROOT TTree format. TTree files are analyzed and energy information for each crystal (sum of the energy information of the two APDs that readout a single crystal), the pulse shape for each input channel as well as the pedestal mean value and RMS extracted.

Fig. 7 shows the typical timing of the analog and digital outputs captured with two Tektronix TDS6804B oscilloscopes (eight channels in total, 500 MSample/s). The trigger was placed in the digital identifier of the first output channel (Channel 0, bottom). The analog outputs (top figure) were shifted 10 clocks for representation purposes in order to appear in phase with the digital identifiers. Power consumption was measured by powering down the “Channel Link” serializer chip, ADCs and corresponding...
LVCMOS-LVDS logic level converters. Measured power consumption at 50 MHz was 660 mW or 3.4 mW per channel, in good agreement with the targeted specifications.

3.2. Pedestal and noise characterization

Quantification of the mean pedestal and chip noise (pedestal RMS) were obtained by reprocessing in off-line mode the dataframes acquired by the L1 trigger. The first pre-sample was extracted from each digital dataframe and binned in different histograms, one per channel. Fig. 8 shows the mean pedestal for 192 channels for one of the two ASICs (results are similar for the other ASIC in the second test board). The mean value was 513 ADC counts. The standard deviation of the baselines among the 192 channels is 2.7 ADC counts (Fig. 9). The dispersion on the mean value is therefore very low, less than 0.5% of the baseline. Since the $V_{th}$ threshold is common to all 192 channels in a single chip, the pedestal stability is a very important parameter since a large inter-channel variation would force the use of a high $V_{th}$ reducing the dynamic range of the chip. Since the adopted ADC is a 10-bit, differential input, from $-1$ to $+1$ V, the 511 ADC count corresponds to 0 V. In this configuration, the standard deviation of the mean pedestal is around 5.4 mV. The result compares well with the predicted 8.6 mV value obtained from dedicated Monte Carlo simulations that take into account process and mismatch variations in the chip production. Regarding the chip noise when
coupled to an LYSO-APD pixel. Fig. 10 presents the pedestal RMS for each of the 192 channels in one chip. The mean value of the noise (Fig. 11) is 2.18 ADC counts (4.4 mV), with a dispersion of 7.8%. For the other chip the mean value was 2.41 ADC counts (4.8 mV) with a similar dispersion. For a 23 mV/fC gain (measured in the second prototype chip which is equipped with the amplifiers of the same topology) this corresponds to an ENC of 1200–1300 e− ENC. In a double readout scheme, the total energy deposited in a crystal is given as

\[ E = E_0 + E_1 \]  

(1)

where \( E_0 \) and \( E_1 \) are the energy collected by the two APD pixels. Therefore two channels from different APDs and ASICs contribute to the total noise. Assuming that the two channels have similar noise and the total noise can be quadratically summed, the noise would be 7 keV (511 keV photopeak at about 200 ADC counts, Section 3.4) which corresponds to a minimum threshold (7 × the noise RMS) of about 50 keV. This result fully supports one of the design goals of the Clear-PEM scanner that is the readout of photon events that undergo in-detector Compton scattering.

### 3.3. Pulse shape

The underlying assumption in the time extraction algorithms running in the L1 and the L2 trigger is that the response of the frontend amplifiers to a characteristic APD input charge can be parameterized by means of a generic function [24]

\[ f(t) = A \left( \frac{T_{\text{max}} - T_{\text{peak}}}{T_{\text{max}}} \right)^x \exp^{-\frac{t - T_{\text{peak}}}{T_{\text{max}}}} \]  

(2)

where \( T_{\text{peak}} \) is the pulse peaking time, \( x \) is a constant, \( T_{\text{max}} \) is the absolute position of the maximum in respect to the sampling clock and \( A \) the amplitude. After \( x \) and \( T_{\text{peak}} \) are computed, \( f(t) \) is used to determine the set of L1 FPGA time filter coefficients or used directly by the pulse fitting algorithms implemented in the L2 trigger [23]. In the Clear-PEM scanner the number of available connections to extract signals at the analog outputs of the frontend chip is limited due to space constrains and low-noise requirements that force a compact PCB layout. The question on how to reconstruct the individual pulse shape for every amplifier was addressed by implementing in the calibration software of the scanner, a module that normalizes the digital dataframe (set of 10 samples readout from the ASIC) by the amplitude of the pulse and computes the estimate of the phase \( \delta_t \), defined as

\[ \delta_t = T_{\text{max}} - \text{MaxClock} \]  

(3)

where MaxClock is the clock position of the highest sample in the dataframe. Each dataframe is then corrected by the phase. After corrected by the time jitter (due to the random nature of the radiation), the samples are accumulated in a profile histogram with a binning between 100 ps and 1 ns, depending on the available statistics. The method was first validated by comparing it against the standard approach which consists on applying a
deviation (corresponding rise time (10–90%) is 30.1 ns with a 0.4 ns standard deviation (extracted from the Gaussian fit), yielding a 3% dispersion. The dispersion is less than 2% (of 57.2 ns with a 1.1 ns standard deviation (extracted from a Gaussian fit) was found. The dispersion is less than 2% (Fig. 14(b)). For a the mean value is 3.5 with a 0.11 standard deviation (extracted from the Gaussian fit), yielding a 3% dispersion. The corresponding rise time (10–90%) is 30.1 ns with a 0.4 ns standard deviation (Fig. 15). The Tpeak and rise time were compared with simulations of the frontend amplifiers, assuming typical process and mismatch variations. A 42 ns LYSO:Ce scintillation light decay time and a Dirac-like response for the APD were assumed. In these simulations of the frontend amplifiers, assuming typical process and mismatch variations, the parameters undertook in order to determine if the slowing down of pulse shape is internal to the chip or is due to some unaccounted capacitance in the PCB or incorrect definition of the LYSO:Ce decay time and APD temporal response.

3.4. Energy measurements

Linear relation between the peak amplitude of the analog data frame (set of samples stored in the memory cells per hit) and the APD charge in 32 of the 192 channels was assessed. An input voltage step amplitude was applied sequentially at an external capacitor by a Tektronics AFG3252 function generator. The external capacitor was needed since the ASIC internal calibration lines were not bonded to the test board PCB. In all 32 channels a good linearity was observed. A linear fit was applied to the amplitude variation as function of the step amplitude and the relative gain measured. Fig. 16(a) shows the distribution of the 32 relative gains. The dispersion (standard deviation/mean) of the relative gains is less than 1.5%. This result is in good agreement with the detailed Monte Carlo simulations of the ASIC, which have yield a dispersion of about 3%. The variation of the mean amplitude of the 32 channels as function of the step voltage is shown in Fig. 16(b). Above a test pulse amplitude of 400 mV the outputs start to saturate, with a significant departure from linearity due to saturation of the amplifiers. No points are shown for test amplitudes less than 100 mV due to limitations of the test setup. The external capacitor was an important source of noise and therefore the Vpeak threshold used to operate the ASIC, in the relative gain measurements, was set at 1.85 V. It should be noticed that the output pulses were recorded with a scope requiring an adaptation from the ASIC differential output channels to 50 Ohm. This reduces the amplitude of the output pulse by about a factor of 10.

Data for all 192 crystals present in the “Trigger Cell” were obtained using 22Na, 137Cs and 176Lu. Fig. 17 shows an occupancy distribution, or number of events above the L1 energy threshold of 200 keV, for acquisitions with 22Na and 176Lu background. Expected the number of decays for the 176Lu acquisition is rather uniform for all crystals. For the 22Na irradiation, three arrays of 32 crystals have a larger number of counts in respect to the neighbor ones, since they are close to the radioactive source. In contrast lower rates were observed for arrays far from the source, since they are shielded by the near modules.

Datstream was analyzed in off-line for the presence of dead channels, linearity and energy resolution. The energy spectra in a typical LYSO:Ce crystal to the 176Lu, 22Na and 137Cs are shown in Fig. 18(a), (b) and (c), respectively. The energy resolution (2.35ΔE/E × 100%), extracted from a Gaussian fit over a linear fit that accounts for the Compton background, at 511 keV for all 192 crystals, is shown in Fig. 19. The distribution is comprehended
between 14% and 19%, with a mean value of 16.8% and a standard deviation of 1.5%. The results are similar to the ones obtained with the Clear-PEM crystal matrices readout by discrete electronics based on CREMAT 110 charge sensitive pre-amplifiers, in which the mean energy resolution and the standard deviation are, respectively, 15.6% and 1.3% [25].

**Fig. 14.** Pulse shape parameters: (a) pulse peaking time $T_{\text{peak}}$ as function of the ASIC readout channel, (b) distribution of $T_{\text{peak}}$ for all 192 channels, (c) $\alpha$ parameter as function of the ASIC readout channel, (d) distribution of $\alpha$ for all 192 channels.

Linearity of the LYSO-APD-ASIC-ADC readout chain was assessed by plotting the reconstructed energy in keV as function of the photopeak position in ADC counts (Fig. 20). A good linearity was found over the entire energy range. At 511 keV the photopeak position is at 195 ADC counts or 390 mV (pulse amplitude). For LYSO:Ce with a decay constant of 40 ns and an amplifier shaping time of 20 ns only 43% of the light contributes to the pulse amplitude, reducing the effective gain to 10 mV/fC, which results in a total charge at 511 keV of 39 fC. Since the APD is operated at a bias supply that at room temperature of $24^\circ\text{C}$ corresponds to a gain 100, the total input charge generated at APD inputs (sum of both APDs) is about 2560 photoelectrons.

In the Clear-PEM scanner the DOI coordinate along the crystal longitudinal axis is determined from the ratio of collected light between the two pixel APDs glued to a given LYSO:Ce 20 mm long crystal:

$$z = c_i \frac{E_0 - E_1}{E_0 + E_1}$$

in which $c_i$ is a calibration constant that translates the light asymmetry to a physical depth, $i$ is the index of the crystal, $E_0$ and $E_1$ are the energy measurements from the two pixel APDs.

A typical distribution of the light collection asymmetry for $^{176}\text{Lu}$ decays in one crystal is shown in Fig. 21. This radioisotope decays through a $\beta^-$ decay followed by a gamma cascade from nuclear de-excitation. Due to the crystal production process it can

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**Fig. 15.** Distribution of pulse rise time (10–90%) for all 192 channels.

**Table:**

<table>
<thead>
<tr>
<th>Rise Time</th>
<th>Entries</th>
<th>Mean</th>
<th>RMS</th>
<th>$\chi^2$/ndf</th>
<th>Prob</th>
<th>Constant</th>
<th>Mean</th>
<th>Sigma</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>192</td>
<td>30.15</td>
<td>0.383</td>
<td>0.00006</td>
<td>0.000</td>
<td>3.915</td>
<td>30.15</td>
<td>0.03</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>
be assumed that the $^{176}$Lu is uniformly distributed throughout the crystal. In this case the $\beta$− decays along the depth direction are distributed symmetrically and the light collection asymmetry distribution should be flat, with the exception of the far edges which correspond to the crystal extremities [26]. As can be observed in Fig. 21, the light collection asymmetry ratio $(E_0 - E_1)/(E_0 + E_1)$ has a dynamic range comprehended between $−60\%$ (interactions near the crystal end at $−10\,\text{mm}$) and $+60\%$ (interactions near the crystal end at $+10\,\text{mm}$). The asymmetry variation per millimeter is therefore of about $6\%\,\text{mm}^{-1}$. This result indicates that the performance of the frontend system is adequate for DOI measurements, since an asymmetry per unit length higher than $4\%\,\text{mm}^{-1}$ are compatible with a DOI resolution of $2.2\,\text{mm}$ FWHM or better [25].

3.5. Time measurements

In most typical exam scenarios in which the Clear-PEM scanner will be used, a significant fraction ($95\%$) of the radioactive activity injected into the patient will be distributed outside the FOV. The scanner will be subject to a flux of single photons up to $2\,\text{MHz}$ per detector head that needs to be discarded as soon as possible in the data acquisition chain, avoiding the introduction of deadtime that could reduce the system efficiency [27]. A good time resolution is also required to minimize the presence of random events through the use of a narrow coincidence window which contribute to a contrast loss and introduction of artifacts in the reconstructed images [28].

Estimates of the time resolution offered by the LYSO-APD-ASIC-ADC assembly were obtained. Time difference taken between the time of the event in the bottom and top APDs that readout the same crystal was computed. Events in the $^{176}$Lu ($306\,\text{keV}$), $^{22}$Na ($511$ and $1275\,\text{keV}$) and $^{137}$Cs ($662\,\text{keV}$) photopeak regions were selected. To avoid introduction of any bias due to the double readout solution, a cut in the asymmetry distribution (Fig. 21) to select events that interacts in the middle of the crystal, from $−10\%$ to $+10\%$, was applied. Experimental results for the time resolution (standard deviation/$\sqrt{2}$) are shown in Fig. 22. The obtained time resolutions were then compared with prior Monte Carlo simulations. The comparison is shown in Fig. 23. The simulations where carried out in the energy range of $100$–$511\,\text{keV}$, well before the chips were delivered from foundry and therefore no tuning on the input parameters was performed [23]. The simulation includes the calculation of the number of collected optical photons in each APD pixel, following the temporal simulation of the LYSO:Ce emission spectra and estimation of the photocurrent produced at the outputs of the APD. Factors such as Poisson fluctuations on the number of generated optical photons and the additional variance in the number of emitted optical photons, given by a constant term independent of the deposited energy were included in the simulation. Fluctuations on total collected charge due to APD excess noise and dark current, variation of quantum efficiency as function of the optical photon wavelength and dependency of gain with quantum efficiency were considered. The main S8550 APD electrical characterization parameters were extracted from Refs. [17,18,29,30]. The chip noise was assumed to be $1300\,\text{e}^−$ ENC. The histogram of the charge pulse is numerical convoluted with the response of the amplifier. The chip shaper response to a Dirac-like pulse is provided as an external input, previously computed from detailed ASIC simulations. At each clock cycle the output pulse is sampled and the corresponding amplitude stored in a $10$ bin-depth vector, emulating the chip analog memories. Simulated dataframes are then processed by a bit-like C++ simulation of the FPGA firmware [31] and fed into the L2 software trigger.

At $511\,\text{keV}$ the experimental single photon time resolution is $1.30\,\text{ns}$, in good agreement with the Monte Carlo value of $1.34\,\text{ns}$. Monte Carlo simulations were also carried out for an ASIC noise of
At 511 keV the single photon time resolution was 1.2 and 1.35 ns, respectively. The weak dependency of the time resolution in this noise range points out that the main factor that limits the time measurement in this energy range is the number of collected photoelectrons before the APD amplification stage, as reported by Ref. [32]. For the same energy deposit, the large fluctuations in the photoelectron yield between events lead to significant pulse shape distortions and additional variability in the peaking time. In this case, the assumption of an invariant \( f(t) \) pulse form will be less accurate effectively limiting further improvements in time resolution.

### 4. Conclusions

In this paper, the overall system design of the Clear-PEM scanner and the key functionalities embedded in an 192-channel ASIC were described as well as the main experimental results. The reported results were obtained in an experimental setup that includes all the main electronics sub-systems developed for the...
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Fig. 22. Experimental time coincidence spectra for events selected in the photopeak region of 306 keV ($^{176}$Lu), 511 keV ($^{22}$Na), 662 keV ($^{137}$Cs) and 1275 keV ($^{137}$Cs).

Fig. 23. Comparison of measured single photon time (RMS) resolution with Monte Carlo simulations as function of the photon energy.

scanner and therefore provide a firm indication of the final performance of the scanner. The frontend chip is characterized by a low-noise (1200–13000 e- ENC), when coupled to pixel APDs with 10 pF capacitance, that should allow to readout events with energies down to 50 keV. Single photon time resolutions are compatible with a 4 ns FWHM coincidence window, essential to minimize the presence of random events. Time as well as the energy resolution are compatible with the reported measurements using discrete electronics which validates the frontend and data acquisition systems design. A very low dispersion between the 192 baselines supports the adoption of a common voltage threshold for the entire chip. In summary, an unprecedented integration of number of APD channels in a high gain and low-noise frontend system was obtained which paves way for the construction of APD pixel-based large scale PET scanners. Based on the experience obtained with the test boards developed for the evaluation of this chip, the final frontend boards that will equip the Clear-PEM scanner were produced. A total of 32 frontend boards with 64 chips were tested. Results are present in Ref. [33].

References
